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Digitale Systeme

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Serie 7

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Presentation tasks

Task

Figure 1 shows a circuit with the inputs $X = (x_0, x_1, x_2)$ and $Y = (y_0, y_1, y_2)$ and the output $E = (e_0, e_1, e_2, e_3, e_4, e_5)$. What does this circuit calculate?
Describe how the circuit works in detail.
Note: The multiplexers used in the figure are simplified. Each of the three multiplexer blocks stands for six multiplexers (one each for e_0 to e_5), which all are being controlled by the same signal of the respective input (x_1 or x_2).

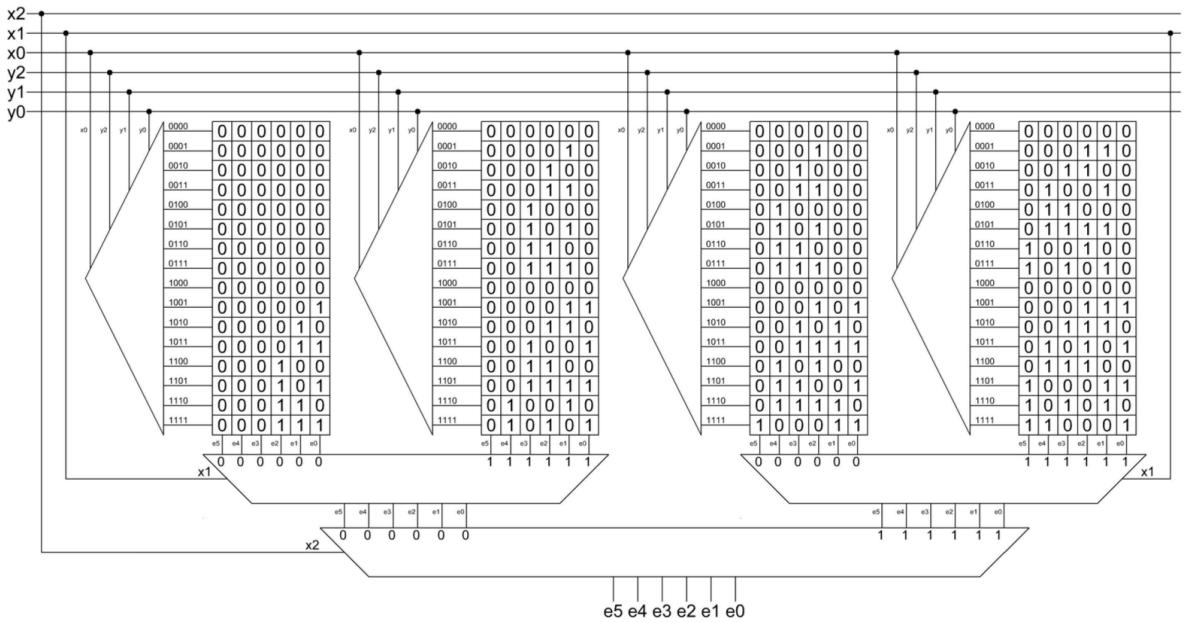

Figure 1

Homework

Task 1

Design a circuit for a 8-Segment Display with the help of the KV diagrams. You know the segment displays from watches with digital display. These have normally a 7-Segment display per digit, with which the numbers 0 to 9 and the letters A to F (B and D in small letters) can be represented. F.W. Wood has patented in 1908 the 8-segment display which has an additional diagonal segment for better representation of the digit 4. Please use the following descriptions for the segments (which are the strokes, of which the digits are grouped together): top: a, left side top segment: b, left side bottom segment: c, bottom: d, right side bottom segment: e, right side top segment: f, middel horizontal: g, additional diagonal element (top half from bottom left to top right): h. The KV diagram shall be described in the same scheme as those in the examples from the script on Chapter 2.6.2, whereby "a" from the script is to be replaced by x_0 , "b" by x_1 etc. Here, $x_n...x_0$ represents the coding vector (please also state in the coding table from x_n (most significant bit, left) to x_0 (least significant bit, right). In the coding table, please first code the numbers incrementing and then the letters (in the consecutive order of the letters).

50 points

Task 2

Design a combinatorial circuit of full adders (FA) and Multiplexers (Mux) that adds 8 binary numbers with the length of 48 bits. The overflows can be neglected here. A full adder and a multiplexer each occupy a chip area of 1 AU (area unit). The switching time of a full adder and a Mux is each 1 TU (time unit). Optimize the circuit in such a way that the product of area A and time T is minimal. Justify your solution. A proof is not necessary.

25 points

Aufgabe 3

Design two CMOS complex gates for the outputs of a full adder. Use as few transistors as possible.

25 points